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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/538,369	06/13/2005	Geoffrey F Burns	US02 0543 US	6028

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P.O. BOX 3001
BRIARCLIFF MANOR, NY 10510

EXAMINER	
FONG, VINCENT	
ART UNIT	PAPER NUMBER
2112	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/21/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/538,369	BURNS ET AL.	
	Examiner	Art Unit	
	Vincent Fong	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 June 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11-25-2005, 06-13-2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the application and amendments filed on 06-13-2005. Claims 1-20 are pending and have been examined.

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 11-25-2005 and 06-13-2005 are being considered by the examiner. Copy of cite No. 4 of IDS filed 6-13-2005 is missing and it is not considered by the examiner.

Drawings

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: element 128 in figure 2 and element 324 in figure 3. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each

drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 13 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Callahan et al. ("The Garp architecture and C compiler", hereinafter Callahan).

As per claim 13, Callahan discloses:

A functional unit (Garp) having a two-dimensional array of processing cells and serving as a component of a main processor (MIPS), the unit having a mechanism for reconfiguring a plurality of intra-processor information paths (programmable wiring) to the array to respective cells on a periphery of the array (side of the control blocks) (Figure 1, page 63 column 1 paragraph 9).

As per claim 19, rejection of claim 13 is incorporated and Callahan further discloses:

An integrated circuit comprising the processor (page 62 column 2 paragraph 1).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1,4,6,7,8,12 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Callahan et al. ("The Garp architecture and C compiler", hereinafter Callahan) in view of Page ("Reconfigurable processors").

As per claim 1, Callahan discloses:

A coprocessor (configurable logic, page 62 column 2 paragraph 6) to a main processor (MIPS, page 62 column 1 paragraph 4) (figure 1),the coprocessor comprising a two-dimensional array of processing cells (page 63 column 1 paragraph 9) and being communicatively connected to said processor by an interface module (control blocks, figure 1) having a mechanism for reconfiguring a plurality of information paths between the interface module and respective cells on a periphery of the array(programmable wiring, page 63 column 1 paragraph 9); control blocks are locate at the side (figure 1) of the array cells.

Callahan does not disclose the coprocessor has a execution speed greater than the processor.

However Page discloses the reconfigurable coprocessor (DPGA XC3195A, page 3 paragraph 4) has a execution speed greater than the processor (T805 RISC processor, page 3 paragraph 4); the DPGA run in the range of 80 Mhz while T805 run in 30 Mhz. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to have make the necessary modification on Callahan's inventions to incorporate Page's inventions. One of ordinary skill in the art would be motivated to make such modification to effectively target the processor in a wide array of applications (page 1 paragraph 2).

As per claim 4, rejection of claim 1 is incorporated and Callahan further discloses: the coprocessor performs mathematical operations whose timing is based on a flow of input operands along the paths (data flow processing, Figure 2c, 3, page 65 column 2 paragraph 1).

As per claim 6, rejection of claim 1 is incorporated and Callahan further discloses: the coprocessor interface module (control blocks) and main processor (MIPS) of claim 1 and a shared memory that communicatively connects with the interface module and the main processor to provide the main processor to coprocessor connection (page 63 column 2 paragraph 2).

As per claim 7, rejection of claim 1 is incorporated and Callahan further discloses:

Coprocessor includes an array processor (Garp array) that comprises said two-dimensional array (2-d array of CLBs, page 63 column 1 paragraph 9).

As per claim 8, rejection of claim 1 is incorporated and Callahan further discloses: An integrated circuit comprising the coprocessor (page 62 column 2 paragraph 1).

As per claim 12, rejection of claim 1 is incorporated and Callahan further discloses: processor comprises a general purpose processor (page 62 column 1 paragraph 4).

As per claim 20, Callahan discloses:
interfacing a coprocessor to a main processor, comprising the steps of: configuring the coprocessor to comprise a two-dimensional array of processing cells (page 62 column 1 paragraphs 3,5); and communicatively connecting the coprocessor to said processor by an interface module (control block, figure 1) having a mechanism for reconfiguring a plurality of information paths (programmable wiring) between the interface module and respective cells on a periphery of the array; control blocks are locate at the side (figure 1) of the array cells.
Callahan does not disclose the coprocessor has a execution speed greater than the processor.
However Page discloses the reconfigurable coprocessor (DPGA XC3195A, page 3 paragraph 4) has a execution speed greater than the processor (T805 RISC processor, page 3 paragraph 4); the DPGA run in the range of 80 Mhz while T805 run in 30 Mhz.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to have make the necessary modification on Callahan's inventions to incorporate Page's inventions. One of ordinary skill in the art would be motivated to make such modification to effectively target the processor in a wide array of applications (page 1 paragraph 2).

8. Claims 2,3,5,10 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Callahan in view of Page further in view of Miyamori et al. ("REMARC: Reconfigurable multimedia array coprocessor", hereinafter Miyamori).

As per claim 2, rejection of claim 1 is incorporated and the combination of Callahan and Page discloses limitation of claim 1.

Neither Callahan nor Page discloses the array comprises a systolic processing array. However Miyamori discloses the array (REMARC, figure 2) comprises a systolic processing array (page 396 column 1 paragraph 2).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to have make the necessary modification on the combination of Callahan and Page to incorporate Miyamori's inventions. One of ordinary skill in the art would be motivated to make such modification to exploit finest grain parallelism efficiently (page 389 column 2 paragraph 3).

As per claim 3, rejection of claim 1 is incorporated and the combination of Callahan and Page discloses limitation of claim 1.

Neither Callahan nor Page discloses the paths are connected one-to-one with said respective cells.

However Miyamori discloses the paths are connected one-to-one (to control unit) with said respective cells (cells on row 0)(figure 2).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to have make the necessary modification on the combination of Callahan and Page to incorporate Miyamori's inventions. One of ordinary skill in the art would be motivated to make such modification to exploit finest grain parallelism efficiently (page 389 column 2 paragraph 3).

As per claim 5, rejection of claim 1 is incorporated and the combination of Callahan and Page discloses limitation of claim 1.

Neither Callahan nor Page discloses inter-cell connection within the array is such that each cell of the array is connected only to cells whose column is the same and whose row is immediately adjacent, and only to cells whose row is the same and whose column is immediately adjacent.

However Miyamori discloses inter-cell connection within the array is such that each cell of the array is connected only to cells whose column is the same and whose row is immediately adjacent, and only to cells whose row is the same and whose column is immediately adjacent (figure 2, page 390 column 2 paragraph 1).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to have make the necessary modification on the combination of Callahan and Page to incorporate Miyamori's inventions. One of ordinary skill in the art would be motivated to make such modification to exploit finest grain parallelism efficiently (page 389 column 2 paragraph 3).

As per claim 10, rejection of claim 1 is incorporated and the combination of Callahan and Page discloses limitation of claim 1.

Neither Callahan nor Page discloses said array is rectangular and said periphery consists of those of said processing cells located in at least one of a first row, last row, first column and last column of said array.

However Miyamori discloses said array is rectangular (8x8 array) and said periphery consists of those of said processing cells (first row, ROW 0) located in at least one of a first row, last row, first column and last column of said array (figure 2, page 390 column 2 paragraph 1).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to have make the necessary modification on the combination of Callahan and Page to incorporate Miyamori's inventions. One of ordinary skill in the art would be motivated to make such modification to exploit finest grain parallelism efficiently (page 389 column 2 paragraph 3).

As per claim 15, rejection of claim 13 is incorporated and see similar rejection of claim 5.

9. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Callahan in view of Page further in view of applicants admitted prior art.

As per claim 9, rejection of claim 8 is incorporated and the combination of Callahan and Page discloses limitation of claim 8.
Neither Callahan nor Page discloses a receiver (mobile phone) comprising the integrated circuit (page 1 lines 19-21).
However Applicant's admitted prior art discloses a receiver comprising the integrated circuit.
It would have been obvious to one of ordinary skill in the art at the time of the invention was made to have make the necessary modification on the combination of Callahan and Page to incorporate applicant's admitted prior art. One of ordinary skill in the art would be motivated to make such modification to adapt to different radio broadcast format (page 1 lines 22-24).

10. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Callahan in view of Page further in view of Taylor (USPN 5857109).

As per claim 11, rejection of claim 1 is incorporated and the combination of Callahan and Page discloses limitation of claim 1.

Neither Callahan nor Page discloses processor comprises a digital signal processor.

However Taylor discloses processor comprises a digital signal processor (Figure 42, column 5 lines 23-26).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to have make the necessary modification on the combination of Callahan and Page to incorporate Taylor's inventions. One of ordinary skill in the art would be motivated to make such modification to provide real time processing power to enhance video output (abstract).

11. Claims 14 and 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Callahan in view of Barat et al. ("Reconfigurable instruction set processor: An implementation platform for interactive multimedia applicaitons", hereinafter Barat).

As per claim 14, rejection of claim 13 is incorporated and Callahan discloses limitations of claim 13.

Callahan does not disclose processor comprises a very long instruction word (VLIW) processor.

However Barat discloses processor comprises a very long instruction word (VLIW) processor (Page 482 column 2 paragraph 2).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to have make the necessary modification on Callahan's inventions to incorporate Barat's inventions. One of ordinary skill in the art would be motivated to make such modification to reduce the execution time of interactive multimedia applications (page 485 column 1 paragraph 2).

As per claim 16, rejection of claim 13 is incorporated and Barat furthers discloses: means for transmitting a plurality of array programs (code) to corresponding predetermined subsets of said processing cells (PE, figure 2); complier generates programs for use in processing cells (page 483 column 2 paragraph 4) and processing cells execute programs (page 482 column 2 paragraph 1) therefore a mean to transfer programs from compiler to processing cells inherently exists.

As per claim 17, rejection of claim 16 is incorporated and Barat further discloses: an array program generator (compiler) for generating the array programs to be transmitted, and, when needed, updating a program (software pipeline, page 483 column 2 paragraph 4), transmitting the updated program, and transmitting concurrently, when needed, a reconfigure signal to said mechanism to correspondingly update a current steady state connection pattern of said information paths (page 483 column 1 paragraph 3), compiler create code and processing cell executing code, it is inherent that the transfer of code form compiler and processing cell exists.

As per claim 18, rejection of claim 17 is incorporated and Barat further discloses: a compiler configured for receiving, in response to said program updating data representative of input and output timing for said unit (timing delay) and further configured for compiling an instruction based on said data (generate code with spatial computation) (page 484 column 1 paragraph 2).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Cooke et al. (USPN 5970254) discloses a system integrated a reconfigurable array with a processor core and connected by a bus.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent Fong whose telephone number is 571-270-1409. The examiner can normally be reached on Monday to Thursday from 7:00 to 4:30. The examiner can also be reached on alternate Friday from 7:00 to 3:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chameli Das can be reached on 571-272-3696. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Vincent Fong VF
December 18, 2006

JEAN M. CORRIELUS
PRIMARY EXAMINER
Art Unit 2162